

SUMMARY:

BSUM(14)

Another . . . means. The variable period oscillator allows the high speed pulses to fill and reset the counter many times before the **variable speed oscillator** stops the counter at a random number. Eventually the clock enables the detection means. If the number contained in the . . .

=> d his

(FILE 'USPAT' ENTERED AT 12:38:01 ON 22 APR 1998)

L1 2263 S (INTEGRAT? (3A) CHIP?)/AB
L2 22 S L1 AND (RING (W) OSCILLATOR?)
L3 0 S L1 AND (VARIABLE (5A) SPEED (5A) RING (W) OSCILLATOR?)
L4 0 S L2 AND (VARIABLE (3A) SPEED)
L5 1 S (VARIABLE (5A) SPEED (5A) RING (5A) OSCILLATOR?)
L6 86 S (VARIABLE (5A) SPEED (5A) OSCILLATOR?)
L7 2 S L6 AND (RING (W) OSCILLATOR?)
L8 0 S L7 AND (ON (W) CHIP?)
L9 0 S L7 AND ON!CHIP
L10 7 S (VARIABLE (W) SPEED (W) OSCILLATOR?)

557705 SPEED
456574. RING
104421 OSCILLATOR?

L5 1 (VARIABLE (5A) SPEED (5A) RING (5A) OSCILLATOR?)

=> d 15 kwic

US PAT NO: 5,530,890 [IMAGE AVAILABLE]

L5: 1 of 1

CLAIMS:

CLMS (7)

7. The microprocessor of claim 1 additionally comprising a **ring oscillator variable speed** system clock connected to said main central processing unit, said main central processing unit and said **ring oscillator variable speed** system clock being provided in a single integrated circuit.

CLAIMS:

CLMS (8)

8. . . . signals, addresses and data with said main central processing unit, said microprocessor additionally including a second clock independent of said **ring oscillator variable speed** system clock connected to said input/output interface.

=> d his

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L1 2263 S (INTEGRAT? (3A) CHIP?)/AB
L2 22 S L1 AND (RING (W) OSCILLATOR?)
L3 0 S L1 AND (VARIABLE (5A) SPEED (5A) RING (W) OSCILLATOR?)
L4 0 S L2 AND (VARIABLE (3A) SPEED)
L5 1 S (VARIABLE (5A) SPEED (5A) RING (5A) OSCILLATOR?)

=> s (variable (5a) speed (5a) oscillator?)

312992 VARIABLE
557705 SPEED
104421 OSCILLATOR?
L6 86 (VARIABLE (5A) SPEED (5A) OSCILLATOR?)

=> s 16 and (ring (w) oscillator?)

456574 RING
104421 OSCILLATOR?
1189 RING (W) OSCILLATOR?
L7 2 L6 AND (RING (W) OSCILLATOR?)

=> d 17 kwic 2

US PAT NO: 5,506,875 [IMAGE AVAILABLE]

L7: 2 of 2

ABSTRACT:

A . . . an incrementor (19) and decrementor (21) and control registers (22). The frequency detector (11) generates an output indicating the relative **speed** of the **variable oscillator** (16) with reference to a externally provided signal. Depending on the output of the frequency detector (11), the arithmetic . . . 21) will increase or decrease the value in a control register (22), resulting in a corresponding increase

or decrease in **speed** of the **variable oscillator** (16). The magnitude of changes in the control register (22) is gradually reduced as the steps of frequency detection and. . .

SUMMARY:

BSUM(11)

Generally, the implementation of a phase-locked loop (PLL) requires the acquisition of an appropriate frequency and phase using an internal **ring oscillator**. Analog phase-locked loops typically use a voltage-controlled oscillator (VCO) to generate a period signal that is "locked" to a reference. . .

SUMMARY:

BSUM(15)

The . . . and phase of an output signal provided by a variable oscillator. A frequency detector generates an output indicating the relative **speed** of the **variable oscillator** with reference to an externally provided reference clock signal. Depending on the output of the frequency detector, arithmetic logic will. . . the control register by a gain value, after each frequency detect cycle, resulting in a corresponding increase or decrease in **speed** of the **variable oscillator**. A controller progressively decreases the magnitude of changes made to the control value after each frequency detect cycle, by dividing. . .

=> s 17 and (on (w) chip?)

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0 ON
131856 CHIP?
0 ON (W) CHIP?
L8      0 L7 AND (ON (W) CHIP?)
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=> s 17 and on!chip

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9 ON!CHIP
L9      0 L7 AND ON!CHIP
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=> d his

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(FILE 'USPAT' ENTERED AT 12:38:01 ON 22 APR 1998)
L1      2263 S (INTEGRAT? (3A) CHIP?)/AB
L2      22 S L1 AND (RING (W) OSCILLATOR?)
L3      0 S L1 AND (VARIABLE (5A) SPEED (5A) RING (W) OSCILLATOR?)
L4      0 S L2 AND (VARIABLE (3A) SPEED)
L5      1 S (VARIABLE (5A) SPEED (5A) RING (5A) OSCILLATOR?)
L6      86 S (VARIABLE (5A) SPEED (5A) OSCILLATOR?)
L7      2 S L6 AND (RING (W) OSCILLATOR?)
L8      0 S L7 AND (ON (W) CHIP?)
L9      0 S L7 AND ON!CHIP
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